PRODUCT INFORMATION LETTER

PIL IPD-PWR/12/7560
Dated 06 Nov 2012

Top Metallization Switch from AlSiCu to AlCu on all LDMOS Technologies

Sales Type/product family label	see attached list
Type of change	Waferfab process change
Reason for change	Product rationalization
Description	Switchover from AlSiCu to AlCu Top Metallization. This change has already successfully been implemented on the STH5P Technology and will be extended to all other less critical LDMOS Technologies (STH1, STH2, STH4, STH5L). Usage of the same metal target on sputtering equipment will avoid changes of targets and consequently longer equipment uptime and availability. As all products involved have metal barrier, the silicon in metal is no more necessary.
Forecasted date of implementation	29-Nov-2012
Forecasted date of samples for customer	30-Oct-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	30-Oct-2012
Involved ST facilities	Catania

DOCUMENT APPROVAL

Name	Function
Juhel, Serge	Marketing Manager
Di giovanni, Filippo	Process Owner
Petralia, Francesco	Q.A. Manager

COMMERCIAL_PRODUCT	FINISHED_GOOD	FORECASTED DATE OF IMPLEMENTATION
PD85035A-E	PD85035A-E$M	Nov'12
PD85035AS-E	PD85035AS-E$M	
PD85035ASTR-E	PD85035ASTR-E$M	
PD20015C	PD20015C$	
PD85025C	PD85025C$	
PD57002-E	PD57002-E$M	
PD55035-E	PD55035-E$M	
PD55035S-E	PD55035S-E$M	
PD55035STR-E	PD55035STR-E$M	
PD57070-E	PD57070-E$M	
PD57070S-E	PD57070S-E$M	
PD54010D2	PD54010D2$1	
PD55025-E	PD55025-E$M	
PD55025S-E	PD55025S-E$M	
PD55025TR-E	PD55025TR-E$M	
PD57060-E	PD57060-E$M	
PD57060S-E	PD57060S-E$M	
PD57060TR-E	PD57060TR-E$M	
PD55003-E	PD55003-E$M	Dec'12
PD55003S-E	PD55003S-E$M	
PD55003TR-E	PD55003TR-E$M	
PD57018-E	PD57018-E$M	
PD57018S-E	PD57018S-E$M	
PD57018STR-E	PD57018STR-E$M	
PD57018TR-E	PD57018TR-E$M	
PD55003L-E	PD55003L-E$	Jan'13
PD54003-E	PD54003-E$M	
PD55008-E	PD55008-E$M	
PD55008S-E	PD55008S-E$M	
PD55008TR-E	PD55008TR-E$M	
PD57030-E	PD57030-E$M	
PD57030S-E	PD57030S-E$M	
LET54008D2	LET54008D2$1	
PD54003L-E	PD54003L-E$	Mar'13
PD55008L-E	PD55008L-E$	
PD54008L-E	PD54008L-E	
PD54008L-E	PD54008L-E$	
PD20015-E	PD20015-E$M	
PD84008-E	PD84008-E$M	
PD84008D1	PD84008D1(9228)	
PD84008D2	PD84008D2$1	
PD84008D2	PD84008D2$2	
PD84008L-E	PD84008L-E$	
PD85025-E	PD85025-E$M	
PD85025S-E	PD85025S-E$M	
PD85025STR-E	PD85025STR-E$M	
PD85025TR-E	PD85025TR-E$M	
PD84010-E	PD84010-E$M	Apr '13
PD84010TR-E	PD84010TR-E$M	
PD85035-E	PD85035-E$M	
PD85035S-E	PD85035S-E$M	
PD85035STR-E	PD85035STR-E$M	
PD85035STR1-E	PD85035STR1-E$M	
PD84001	PD84001$	May'13
PD54008-E	PD54008-E$M	
PD54008D2	PD54008D2$1	
PD54008S-E	PD54008S-E$M	
PD54008TR-E	PD54008TR-E$M	
PD55015-E	PD55015-E$M	
PD55015S-E	PD55015S-E$M	
PD55015STR-E	PD55015STR-E$M	
PD55015TR-E	PD55015TR-E$M	
PD57045-E	PD57045-E$M	
PD57045TR-E	PD57045TR-E$M	
PD57006-E	PD57006-E$M	July'13
PD57006S-E	PD57006S-E$M	
PD57006STR-E	PD57006STR-E$M	
PD57006TR-E	PD57006TR-E$M	

Reliability Evaluation Report on
Extension of STH5P improvements to all LDMOS

General Information	
Product Line	*A580*
Product Description	*RF power transistor*
P/N	*PD85035A-E*
Product Group	*IPD*
Product division	*POWER TRANSISTORS Power RF*
Package	*PowerSO-10 R.F. (gull wing)*
Silicon Process technology	*LDMOS STH5*
Production mask set rev	NSE011-C
Maturity level step	*30*

Locations	
Wafer fab	*CATANIA*
Assembly plant	*MUAR*
Reliability Lab	*CATANIA Reliability Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	13-Jun-2012	7	A.Riciputo	G.Presti	First Release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
RER.325W.10	Reliability Report on LDMOS STH5P technology qualification

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To extend STH5P improvements on all LDMOS

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Common source N-channel enhancement-mode lateral field-effect RF power transistor.

4.2 Construction note

	PD85035A-E
Wafer/Die fab. information	
Wafer fab manufacturing location	CATANIA
Technology	LDMOS STH5
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	5200, 1090 micron
Bond pad metallization layers	AlCu
Wafer Testing (EWS) information	
Electrical testing manufacturing location	CATANIA
Tester	T84
Assembly information	
Assembly site	MUAR
Package description	PowerSO-10 R.F. (gull wing)
Molding compound	SUMITOMO EME-G700LS
Frame material	PSO-10 RF Mtx formed leads SpAg
Die attach process/material	Hard / Au Eutectic
Wires bonding materials/diameters	Au/ 1.2mils
Final testing information	
Testing location	ST-BSK Casablanca
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Technical Code	Package	Product Line	Comments
1	Y121096 (wfrs:#09, #04, #12)	TM3H*A5800Y4	PSO10	A580	

5.2 Test plan and results summary

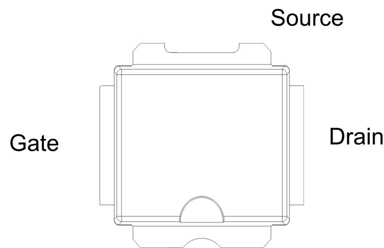
PD85035A-E

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
						Lot 1	
Die Oriented Tests							
HTRB	N	JESD22 A-108	Tj = 150°C, +32V	77	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTSL	N	JESD22 A-103	Ta = 175°C	45	168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 40 H @ Ta=60°C Rh=60% Over Reflow @ Tpeak=250°C 3 times		Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, +24V	77	168 H	0/77	
					500 H	0/77	
					1000 H	0/77	

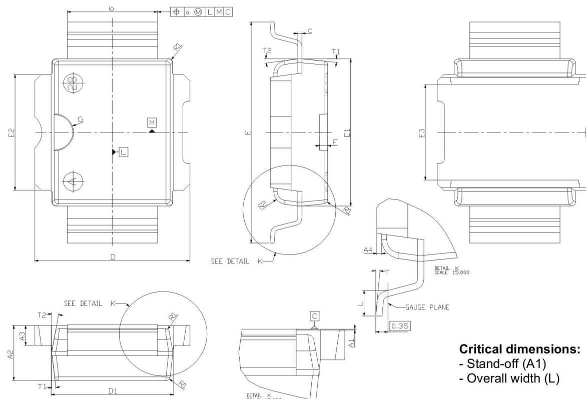
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Package outline/Mechanical data



Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A1	1.62	1.67	1.72	0.064	0.065	0.068
A2	3.4	3.5	3.6	0.134	0.137	0.142
A3	1.2	1.3	1.4	0.046	0.05	0.054
A4	0.15	0.2	0.25	0.005	0.007	0.009
a		0.2			0.007	
b	5.4	5.53	5.65	0.212	0.217	0.221
c	0.23	0.27	0.32	0.008	0.01	0.012
D	9.4	9.5	9.6	0.370	0.374	0.377
D1	7.4	7.5	7.6	0.290	0.295	0.298
E	15.15	15.4	15.65	0.595	0.606	0.615
E1	9.3	9.4	9.5	0.365	0.37	0.375
E2	7.3	7.4	7.5	0.286	0.292	0.294
E3	5.9	6.1	6.3	0.231	0.24	0.247
F		0.5			0.019	
G		1.2			0.047	
R1			0.25			0.01
R2		0.8			0.031	
T1		6 deg			6 deg	
T2		10 deg			10 deg	

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias **HTFB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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